AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-9 (Cancelled)

10. (New) An integrated semiconductor apparatus comprising:

at least one fuse box device comprising fuses for storing trimming data, a fuse box trimming output, and a timer emitting a clock signal;

a parallel/serial converter connected to the fuses and to the timer; the parallel/serial converter being configured to read, in parallel, the trimming data from the fuses and to emit, in serial, the trimming data from the fuse block trimming output based on the clock signal;

generators, each generator generating a generator signal, each generator comprises:

a trimming unit having a trimming signal input, the trimming unit being configured to trim the generator signal of the generator based on the trimming data received;

a trimming signal output;

memory flip-flops connecting the trimming input signal to the trimming output signal; and

wherein each of the memory flip-flops connects each trimming unit to the fuse block trimming output to form a shift register chain for serial transmission of the trimming data from the at least one fuse block device to the generators.

11. (New) The apparatus of claim 10, wherein the trimming signal input is connected from one of the generators to the fuse block trimming output; and

wherein the trimming signal inputs of the other generators are each connected in a chain to one of the trimming signal outputs.

12. (New) The apparatus of claim 10, wherein each generator is a voltage generator and the generator signal is an output voltage, and wherein the trimming unit trims the output voltage based on the trimming data.

13. (New) The apparatus of claim 10, wherein the generator is a delay generator and wherein the generator signal is a time-delayed signal, and wherein the trimming unit trims the time delay of the time-delayed signal based on the trimming data.

14. (New) The apparatus of claim 10, wherein each generator further comprises a clock input; and wherein the fuse block device further comprises a fuse block clock output for emitting the clock signal from the timer to the clock input of each generator.

15. (New) The apparatus of claim 10, wherein the parallel/serial converter emits pulse-width modulated trimming data.

16. (New) The apparatus of claim 10, wherein the fuses are electrically-programmable.

17. (New) The apparatus of claim 10, wherein the fuses are laser-programmable.

18. (New) The apparatus of claim 10, wherein the integrated semiconductor apparatus comprises an integrated semiconductor memory.

19. (New) The apparatus of claim 10, wherein the integrated semiconductor apparatus comprises an integrated logic circuit.

20. (New) A method of trimming generator signals generated from generators, comprising:

reading, in parallel, stored trimming data for generators;

connecting to each generator to form a shift register chain for serial transmission of the trimming data to the generators;

emitting, in serial, the trimming data based on a clock signal; and

trimming each generator signal based on the trimming data received.

21. (New) The method of claim 20, wherein each generator comprises a trimming signal input and a trimming signal output, and further comprising;

connecting trimming data to the trimming data input of one of the generators; and

connecting, in a chain, the trimming signal inputs of the other generators to one of the trimming signal outputs.

22. (New) The method of claim 20, wherein each generator is a voltage generator and the generator signal is an output voltage, and wherein trimming the generator signal comprises trimming the output voltage based on the trimming data.

23. (New) The method of claim 20, wherein the generator is a delay generator and wherein the generator signal is a time-delayed signal, and wherein trimming the generator signal comprises trimming the time delay of the time-delayed signal based on the trimming data.

24. (New) The method of claim 20, further comprising sending the clock signal to each generator.

25. (New) The method of claim 20, wherein emitting comprises emitting pulse-width modulated trimming data.

26. (New) The method of claim 20, wherein the fuses are electrically-programmable.

27. (New) The method of claim 20, wherein the fuses are laser-programmable.

28. (New) The method of claim 20, wherein the integrated semiconductor apparatus comprises an integrated semiconductor memory.

29. (New) The method of claim 20, wherein the integrated semiconductor apparatus comprises an integrated logic circuit.